CLAIMS

What is claimed is:

1. A crystallization method of an amorphous silicon thin film, the method comprising:

forming a black matrix layer to absorb external light on a substrate, an upper region of the black matrix layer having a catalyst for crystallization;

patterning the black matrix layer;

forming the amorphous silicon thin film on the substrate and the black matrix layer; and

thermally processing the amorphous silicon thin film for crystallization.

2. The crystallization method of claim 1, wherein:

the forming of the black matrix layer comprises forming a functional thin film having a transparent first component in a lower region thereof facing the substrate and a metallic second component in an upper region thereof, and

the forming of the functional thin film includes forming the transparent first component having a gradually decreasing concentration and the metallic second component having a gradually increasing concentration, with increasing distance from the substrate.

3. The crystallization method of claim 2, wherein the transparent first component comprises at least one selected from the group consisting of SiO_x where $x \geq 1$, SiN_x where $x \geq 1$, MgF_2, CaF_2, Al_2O_3, and SnO_2, and the group consisting of ITO, IZO, ZnO, and In_2O_3.

4. The crystallization method of claim 2, wherein the metallic second component comprises at least one metal selected from the group consisting of Fe, Co, V, Ti, Al, Ag, Si, Ge, Y, Zn, Zr, W, Ta, Cu, and Pt.

5. The crystallization method of claim 1, wherein the black matrix layer comprises a CrO_x thin film where $x \geq 1$, or a Cr thin film.

6. The crystallization method of claim 1, wherein the forming of the black matrix layer comprises:

forming a functional thin film having a first thin film formed of CrO_x, where $x \geq 1$, on the substrate; and

forming a second thin film formed of Cr on the first thin film.

7. The crystallization layer of claim 1, wherein:

the black matrix layer is for a flat panel display, and

the patterning of the black matrix layer comprises patterning the black matrix layer simultaneously with a patterning operation to expose a pixel region of the flat panel display.

8. The crystallization method of claim 1, wherein the catalyst is a catalyst for silicon crystallization comprising at least one selected from the group consisting of Ni, Pd, Au, Sn, Sb, Cr, Mo, Tr, Ru, Rh, Fe, Co, V, Ti, Al, Ag, Cu, and Pt.

9. A crystallization method of an amorphous silicon thin film, the method comprising:

forming a black matrix layer to absorb external light on a substrate;

forming a crystallization thin film having a catalyst for crystallization on the black matrix layer;

patterning the black matrix layer and the crystallization thin film;

forming the amorphous silicon thin film on the substrate and the patterned crystallization thin film; and

thermally processing the amorphous silicon thin film for crystallization.

10. The crystallization method of claim 9, wherein:

the forming of the black matrix layer comprises forming a functional thin film having a transparent first component in a lower region thereof facing the substrate and a metallic second component in an upper region thereof, and

the forming of the functional thin film includes forming the transparent first component having a gradually decreasing concentration and the metallic second component having a gradually increasing concentration, with increasing distance from the substrate.

11. The crystallization method of claim 10, wherein the transparent first component comprises at least one selected from the group consisting of SiO_x where $x \geq 1$, SiN_x where $x \geq 1$, MgF_2, CaF_2, Al_2O_3, and SnO_2, and the group consisting of ITO, IZO, ZnO, and In_2O_3.

12. The crystallization method of claim 10, wherein the metallic second component comprises at least one metal selected from the group consisting of Fe, Co, V, Ti, Al, Ag, Si, Ge, Y, Zn, Zr, W, Ta, Cu, and Pt.

13. The crystallization method of claim 9, wherein the black matrix layer comprises a CrO_x thin film where $x \geq 1$, or a Cr thin film.

14. The crystallization method of claim 9, wherein the forming of the black matrix layer comprises:

forming a functional thin film having a first thin film formed of CrO_x, where $x \geq 1$, on the substrate; and

forming a second thin film formed of Cr on the first thin film.

15. The crystallization method of claim 9, wherein:

the black matrix layer is for a flat panel display, and

the patterning the black matrix layer comprises patterning the black matrix layer simultaneously with a patterning operation to expose a pixel region of the flat panel display.

16. The crystallization method of claim 9, wherein the catalyst is a catalyst for silicon crystallization comprising at least one selected from the group consisting of Ni, Pd, Au, Sn, Sb, Cr, Mo, Tr, Ru, Rh, Fe, Co, V, Ti, Al, Ag, Cu, and Pt.

17. A thin film transistor comprising:

a substrate;

a semiconductor active layer having channel, source and drain regions formed on the substrate, wherein:

the source and drain regions are formed at respective sides of the channel region, and

at least the channel region is formed as a metal-induced lateral crystallization (MILC) region;

a black matrix layer interposed between the substrate and at least the source region and the drain region of the semiconductor active layer, wherein an upper region of the black matrix layer includes a catalyst for crystallization;

a gate dielectric layer formed on the channel region; and

a gate electrode formed on a gate dielectric layer.

18. The thin film transistor of claim 17, wherein:

the black matrix layer is a functional thin film having a transparent first component in a lower region thereof facing the substrate and a metallic second component in an upper region thereof, and

the transparent first component has a gradually decreasing concentration and the metallic second component has a gradually increasing concentration, with increasing distance from the substrate.

19. The thin film transistor of claim 18, wherein the transparent first component comprises at least one selected from the group consisting of SiO_x where $x \geq 1$, SiN_x where $x \geq 1$, MgF_2, CaF_2, Al_2O_3, and SnO_2, which are transparent insulating materials, and the group consisting of ITO, IZO, ZnO, and In_2O_3, which are transparent conductive materials.

20. The thin film transistor of claim 18, wherein the metallic second component comprises at least one metal selected from the group consisting of Fe, Co, V, Ti, Al, Ag, Si, Ge, Y, Zn, Zr, W, Ta, Cu, and Pt.

21. The thin film transistor of claim 17, wherein the black matrix layer comprises a CrO_x thin film where $x \geq 1$, or a Cr thin film.

22. The thin film transistor of claim 17, wherein the black matrix layer is a functional thin film comprising a first thin film formed of CrO_x, where $x \geq 1$, on the substrate and a second thin film formed of Cr on the first thin film.

23. The thin film transistor of claim 17, wherein the catalyst is a catalyst for silicon crystallization comprising at least one selected from the group consisting of Ni, Pd, Au, Sn, Sb, Cr, Mo, Tr, Ru, Rh, Fe, Co, V, Ti, Al, Ag, Cu, and Pt.

24. The thin film transistor of claim 17, wherein the black matrix layer slopes downward from the source region and the drain region toward the channel region.

25. The thin film transistor of claim 24, wherein:

each of the source region and the drain region includes a combined region facing the channel region and a metal-induced crystallization (MIC) region, and

the combined region includes a portion of the MILC region and a portion of the MIC region.

26. The thin film transistor of claim 17, further comprising a silicon crystallization catalyst thin film comprising at least one metal selected from the group consisting of Ni, Pd, Au, Sn, Sb, Cr, Mo, Tr, Ru, Rh, Fe, Co, V, Ti, Al, Ag, Cu, and Pt, which is provided between the black matrix layer and the source and drain regions.

27. A flat panel display comprising:

an insulating substrate;

a pixel region including pixels arranged in a matrix on the insulating substrate; and

at least one thin film transistor near the pixel region, wherein the at least one thin film transistor comprises:

a semiconductor active layer having channel, source and drain regions fromed on the insulating substrate, the source and drain regions formed at respective sides of the channel region, wherein at least the channel region is formed as a metal-induced lateral crystallization (MILC) region,

a gate dielectric layer formed above the channel region,

a gate electrode formed on the gate dielectric layer, and

a black matrix layer interposed between the insulating substrate and the gate dielectric layer, the black matrix layer having an opening which exposes at least the channel region between the source region and the drain region of the semiconductor active layer and an opening which exposes the pixel region.

28. The flat panel display of claim 27, wherein the black matrix layer slopes downward from the source region and the drain region toward the channel region.

29. The flat panel display of claim 28, wherein:

each of the source region and the drain region includes a combined region facing the channel region and a metal-induced crystallization (MIC) region, and

the combined region includes a portion of the MILC region and a portion of the MIC region.

30. The flat panel display of claim 27, wherein an upper region of the black matrix layer facing the semiconductor active layer comprises at least one metal selected from the group consisting of Ni, Pd, Au, Sn, Sb, Cr, Mo, Tr, Ru, Rh, Fe, Co, V, Ti, Al, Ag, Cu, and Pt.

31. The flat panel display of claim 27, further comprising a silicon crystallization catalyst thin film comprising at least one metal selected from the group consisting of Ni, Pd, Au, Sn, Sb, Cr, Mo, Tr, Ru, Rh, Fe, Co, V, Ti, Al, Ag, Cu, and Pt, which is provided between the black matrix layer and the source and drain regions of the semiconductor active layer.

32. The thin film transistor of claim 17, wherein the black matrix layer is a functional thin film having a transparent first component in a lower region thereof facing the substrate and a metallic second component in an upper region thereof, except an area of the functional thin film underneath the channel region does not comprise the metallic second component.

33. The thin film transistor of claim 17, wherein the back matrix comprises a plurality of thin films which are sequentially stacked in an order of their refractive indices so as to increasingly vary a light absorption coefficient of the black matrix along a thickness thereof.

34. The thin film transistor of claim 25, wherein the MIC region and the MILC region are formed to be continuous without a definite boundary therebetween.

35. The flat panel display of claim 27, wherein the flat panel display further comprises:

an interlayer insulating layer formed on the gate electrode and the gate dielectric layer;

source and drain electrodes which are formed on the interlayer insulating layer and electrically connected to the source and drain regions, respectively, of the semiconductor active layer; and

a passivation layer formed on the interlayer insulating layer, the source electrode, and the drain electrode so as to connect a pixel electrode of the pixel region to the drain electrode.

36. The flat panel display of claim 27, wherein the opening which exposes the at least the channel region and the opening which exposes the pixel region are simultaneously formed through a single patterning operation.